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(54) Matrix display device with light sensing function

Matrixanzeigevorrichtung mit lichtempfindlichen Elementen

Dispositif d'affichage matriciel avec éléments sensibles à la lumière

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EP-A- 0 491 436
US-A- 4 345 248

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Description

[0001] This invention relates to a matrix display device for displaying information which includes optical sensing means for enabling input of information as well, for example by way of a light pen. More particularly, the invention relates to a combined matrix display and light sensing device comprising an array of display elements, an array of light sensing elements which are responsive to illumination so as to provide an electrical charge indicative thereof, first and second sets of address conductors connected with the arrays of display and light sensing elements, the display elements and the light sensing elements each being connected with an address conductor of each set, a first drive circuit connected to the first set of address conductors for scanning the arrays, a second drive circuit for providing data signals which are supplied to the display elements via address conductors of the second set, a detection circuit for sensing the charge provided by the sensing elements and providing an output in accordance therewith and comprising charge sensitive amplifier circuits each having an output, a first input connected to an address conductor of the second set, a second input for receiving a read potential and a capacitor and switch connected in parallel between the output and the first input, and control means for opening and closing the switch of each charge sensitive amplifier circuit periodically and providing a read potential to the second input.

[0002] This kind of device may be used for example as an output/input interface for a computer system through which information can be displayed to a user and information entered by a user by writing with a light pen.

[0003] An example of such a device is described in EP-A-0491436. This device comprises a row and column array of liquid crystal display elements, each of which includes a switching element in the form of a thin film transistor (TFT), combined with a row and column array of light sensing elements which each comprise a photo-sensitive element, for example a photo-diode or photo-resistor, connected to a capacitor and a switching element, also comprising a TFT. The TFTs of the display elements and the sensing elements are connected to row and column address conductors. The display elements are driven in conventional fashion by a scan drive circuit which applies a selection signal to each row conductor in turn, and a data signal drive circuit which applies display data signals to the column conductors. The data signal drive circuit can be of a conventional kind used in matrix display devices comprising a sample and hold circuit operated by a shift register to perform serial to parallel conversion of a serial data signal input. A sampled data signal is supplied to a column of display elements via a column address conductor by a respective stage of the sample and hold circuit. It is common in such data signal drive circuits for the sampled data signals to be fed to the column address conductor via respective buffer amplifiers.

[0004] The display and sensing elements share the same row and column address conductors with an associated pair of display and sensing element conductors being connected to a respective column address conductor. A row selection signal provided by a scan drive circuit defines a row address period during which display information is written into a row of display elements and a read out is provided from the associated row of sensing elements. A charge is periodically applied to the capacitors of the sensing elements and this charge is changed in the intervening periods if the photosensitive element is illuminated. The charge state of the capacitors is monitored to provide an indication of whether or not the sensing elements have been illuminated by means of a detection circuit which includes for each column of sense elements a respective a charge sensitive amplifier circuit connected to a column address conductor providing a read-out in accordance with the charge state of the sensing elements.

[0005] The use of charge sensitive amplifier circuits for providing a read-out from an array of light sensitive elements follows known practice in matrix light sensing devices, without a display function, for example as described in EP-A-0237365 and EP-A-0233104.

[0006] A combined matrix display and light sensing device is described in US-A-4345248 in which arrays of display and light sensing elements are addressed via the same sets of row and column electrodes and a column electrode drive and detection circuit that is switched to apply data signals to the column electrodes in a display field and to detect sensing element outputs via the column electrodes in a detection field.

[0007] It is an object of the present invention to provide an improved combined matrix display and light sensing device in which the required drive circuitry is simplified.

[0008] According to the present invention there is provided a combined matrix display and light sensing device of the kind described in the opening paragraph which is characterised in that the control means is operable to apply to the second input of each charge sensitive amplifier circuit data signals from the second drive circuit when the switch is closed and said read potential when the switch is open. With this arrangement, therefore, a single amplifier circuit is utilised to perform the role of a charge sensitive amplifier in the detection circuit and also the role of a buffer amplifier in the data signal drive circuit. The invention stems from the recognition that both functions can be performed conveniently with a single amplifier circuit in time sharing manner. With the switch of the sense amplifier circuit in its closed state, a data signal applied to the second input appears on an associated address conductor of the second set, and can then be transferred to a selected display element in the usual manner. With the switch in its open state and with a read potential applied to the second input the charge sensitive amplifier circuit behaves in con-

ventional manner to provide a read-out from a selected sensing element. The peripheral drive circuitry for the arrays of display and sensing elements is thus considerably simplified with the number of components required being significantly reduced. An additional and advantageous consequence of this simplification is that the drive circuitry consumes less power.

[0009] In one embodiment of the device, individual address conductors of the second set may be connected to display elements and sensing elements, as in the arrangement described in EP-A-0491436, in which case the individual address conductors are each connected to the first input of a respective charge sensitive amplifier circuit. Such sharing of the address conductors of the second set by the display and sensing elements minimises the number of address conductors required and simplifies construction. However, it may be preferred in some situations to use separate address conductors for the sensing and display elements respectively, for example to allow the sensing and display elements to be operated more independently. In another embodiment, therefore, the display elements and sensing elements may be connected respectively to different ones of the second set of address conductors in which case a pair of address conductors of the second set comprising one connected to display elements and one connected to sensing elements may be connected to the first input of a respective charge sensitive amplifier circuit via a change-over switch operable by the control means in synchronism with the switch of the sense amplifier circuit.

[0010] Embodiments of a combined matrix display light sensing device in accordance with the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a schematic diagram of one embodiment of combined matrix display and light sensing device according to the present invention;

Figure 2 is a schematic circuit diagram of a typical display element and light sensing element combination of the device;

Figure 3 shows schematically a single stage of a sense circuit of the device of Figure 1;

Figure 4 shows schematically a single stage of a modified sense circuit in a second embodiment of combined matrix display and light sensing device according to the present invention, and

Figure 5 shows schematically the circuit of an alternative form of light sensing element.

[0011] It should be understood that the Figures are merely schematic and are not drawn to scale. In particular certain dimensions may have been exaggerated whilst other dimensions may have been reduced. It should also be understood that the same reference numerals are used through the Figure to indicate the same or similar parts.

[0012] Referring to Figure 1, the device comprises a panel 10 having combined row and column arrays of actively addressed liquid crystal display elements 12 and light sensing elements 18 with sets of row and column address conductors 14 and 16, and peripheral drive circuitry comprising a scan signal drive circuit 15 connected to the row address conductors 14, a column drive/read circuit 17 connected to the column address conductors and a control circuit 19 which controls the timings of the operations of the circuits 15 and 17 and supplies operating voltages and a video signal providing display data signals for the display elements. With the exception of the column drive/read circuit 17, and to an extent the control circuit 19, the device is similar in many respects to that described in EP-A-0491436 whose disclosure is therefore incorporated herein by reference. In particular the panel 10 and the manner of its operation generally corresponds and consequently the description of these aspects will be kept brief. For further information, the reader is invited to refer to the aforementioned patent specification.

[0013] The panel 10 has m rows of display elements with n horizontally arranged display elements in each row. Each display element 12 is located at a respective intersection between crossing sets of m row address conductors 14 and n column address conductors 16. Only a few of the display elements are shown in Figure 1, for clarity. A sensing element 18, is located adjacent each display element 12, except for the first column of display elements, giving a high resolution sensing capability. The circuit of one typical pair of display and sensing elements is shown in Figure 2. Each display element 12 includes a thin film field effect transistor, TFT, 20 connected with a liquid crystal element 21, represented by a capacitor. The gates of all TFTs 20 of the display elements in one row are connected to a respective one of the row address conductors 14. The sources of all TFTs 20 of picture elements in one column are connected to a respective one of the column address conductors 16. The drain terminals of the TFTs 20 are connected to a first electrode 22 of their associated LC elements 21. The sets of row and column address conductors 14 and 16, the TFTs 20, and the LC element first electrodes 22 are all carried on a supporting plate of transparent insulating material, for example glass. The panel 10 further comprises a second transparent supporting plate arranged parallel to, and spaced from, this supporting plate with twisted nematic LC material contained therebetween. This second plate carries a continuous transparent conductive layer constituting an electrode, 23, common to all LC display elements. The two opposing plates are provided internally with orientation layers and externally with polarising layers in the usual manner for LC display devices.

[0014] Each sensing element 18 includes a TFT 24. The sensing elements share the same address conductors as the display elements with the gates of all TFTs 24 in a row being connected to a respective one of the

row address conductors 14 and with the sources of all TFTs 24 in a column being connected to a respective one of the column address conductors 16. The source of the TFT 24 is connected to one side of charge storage capacitor 25 whose other side is connected to an adjacent row address conductor 14 associated with the next row of display and sensing elements. In an alternative arrangement the other sides of the capacitors 25 may instead be connected to a dedicated auxiliary row conductors as described in EP-A-0491436. In a further alternative arrangement, the source of the TFT 24 may be connected to the same column address conductor 16 as the TFT 20 rather than the adjacent column conductor associated with the preceding column of display elements as shown.

[0015] The sensing element 18 includes a photosensitive element 26, constituted by a photoresistor, which is connected across the capacitor 25 between the drain of the TFT 24 and the next row address conductor 14 (or auxiliary row conductor if used). The photosensitive elements can comprise other forms of photo conductive devices which exhibit an increase in conductance in response to being illuminated, for example photodiodes, as also described in EP-A-0491436.

[0016] In this particular embodiment the TFTs 20 and 24 comprise hydrogenated amorphous silicon TFTs, and the photo-resistors 26 comprise amorphous silicon material.

[0017] Referring again to Figure 1, the scan signal drive circuit 15 is of a kind conventionally used in TFT matrix display devices and comprises a digital shift register whose operation is controlled by timing signals provided by the control circuit 19 and which sequentially addresses the row conductors 14 with a selection (scan) signal on a row at a time basis. The drive circuit 15 applies a selection signal to each row address conductor 14 in turn, and holds each conductor 14 at a reference potential level in the interval between successive selection signals, corresponding to a field period.

[0018] The column drive/read circuit 17 operates to apply data signals to the array of display elements so a to produce the required display effect from the panel and also to monitor light inputs applied to the array of sensing elements and provide an indication in accordance therewith. To this end the circuit 17 comprises a data signal drive circuit 30 similar to those commonly used in TFT display devices and consisting of a sample and hold circuit operated by a shift register to perform serial to parallel conversion of a video signal supplied in serial form from the control circuit 19. Data signals for each row of display elements in turn are provided by the circuit 30 to the column address conductors 16 in synchronism with the selection signals applied to the row address conductors 14. Data signal drive circuits of this kind are well known in the field of matrix liquid crystal display devices and accordingly will not be described here in detail.

[0019] The circuit 17 further includes a detection circuit 40 which comprises a set of charge sensitive amplifiers, one for each column conductor, whose function is to provide an output indicative of the state of the sensing elements 18, that is, according to whether or not they have been illuminated, for example by means of a light pen referenced at 41 in Figure 1. The charge state of a sensing element's capacitor 25, e.g. the level of the charge stored in a capacitor 25, is dependent on whether or not the associated photosensitive element 26 has been illuminated. The detection circuit periodically addresses the capacitors 25 to sense their charge state and provides an output in accordance therewith indicating whether or not the sensing elements have been subjected to illumination in the interval between successive addressing. Movement of the light pen 41, which consists of a light source which continuously emits light in operation, over the display panel results in sensing elements located under its path of travel being illuminated. The detection of those illuminated sensing elements, representing the pattern of the light pen movement, enables data or information to be written into the device.

[0020] The arrays of display and sensing elements of the panel 10 are operated in a manner similar to that described in EP-A-0491436 to which reference is invited for details. Briefly, each selection signal supplied to a row address conductor defines a row selection period and turns on the TFTs 20 and 24 of the display and sensing elements in the row concerned for the duration of this period. For the remainder of a field period the TFTs are held off by a lower, non-selection reference level applied by the circuit 15 to the row address conductor. During a first part of a selection signal, a suitably selected reference potential level, constituting a "read" potential as will become apparent, is applied to the column conductors 16 and during a latter part of the selection signal the data signals provided by the data signal drive circuit 30 are applied to the column conductor 16 and consequently loaded into the display elements of that row. Similarly, the capacitors 25 of the sensing elements of that row are also charged according to the level of the applied data signals and also the level of the non-selection potential then being applied to the other side of the capacitors 25.

[0021] Following termination of the row selection signal the TFTs 24, like the TFTs 20, of that row are turned off, thereby isolating the capacitors 25, until the row of sensing elements is next addressed in the subsequent field period. When next addressed with a row selection signal the TFTs 20 and 24 of the display elements and sensing elements of the row are again turned on and the potential of the column conductors 16 during this first part of the row selection signal is similarly set to the selected reference level. Depending on the level of charge then existing on the capacitors 25 a charging current will flow through the conductors 16 to charge the capacitors 25 (and the display elements 21) to the column conductor voltage. The sensitivity of the photosensitive elements 26 of the elements 18 is chosen so that under

normal ambient illumination the capacitors 25 are not discharged to any significant extent and accordingly very little charging current flows during this period in the case where the photosensitive elements have been subjected only to ambient illumination in the preceding field period.

[0022] If during the preceding field period a sensing element 18 has been "written" with the light pen 41 then the comparatively high light intensity will have caused the photosensitive element 26 of the sensing element 18 to conduct heavily, thus substantially discharging the capacitor 25 so that an appreciable charge will flow into its capacitor 25.

[0023] The charge sensitive amplifiers of the detection circuit 40 connected to respective column conductors 16, are responsive to the charges supplied to the capacitors 25 in this period. After amplification in the sensing amplifiers the signals produced as a result of the recharging of the capacitors 25 are passed to a threshold circuit of the detection circuit 40 whose output switches state if the signal level exceeds a predetermined value which is set to lie between that produced by a "written" and an "unwritten" sensing element. The reference, read, level applied to the column conductors is selected such that the polarity of the charging signals for written and unwritten sensing elements will be opposite, which can make discrimination between them easier. The output obtained from the circuit 40 is passed to the control circuit 19.

[0024] The detection circuit 40 will now be described with reference to Figure 3 which illustrates schematically the circuit of one typical stage of the detection circuit 40 associated with a respective column conductor 16, the circuit 40 having identical stages for other column conductors. The stage consists of a charge sensitive amplifier circuit 45 comprising an operational amplifier 46 with a capacitor 47 and a switch 48 connected in parallel between its inverting input and its output in conventional manner. The output and inverting input are connected respectively to a multiplexer 50 and the column conductor 16. The non-inverting input of the amplifier is connected to a change over switch 51. The switches 48 and 51 are operable under the control of switching signals supplied by the control circuit 19. During the first part of a selection signal applied to a row conductor 14, the switch 48 is opened and the switch 51 set to the position illustrated in which reference "read" potential level, here designated Vread, is applied to the amplifier's non-inverting input. Charging current for the capacitor 25 of the selected sensing element associated with the column conductor 16 is then integrated by the sense amplifier circuit 45. The resulting output voltage from this read operation appears at the output of the operational amplifier 46 and is supplied, along with the outputs from the operational amplifiers of the other stages, to the multiplexer 50 from which a serial output of signals representing the charge states of the capacitors of the selected row of sensing elements is obtained in the interval between successive row selection signals. Readout of the charge sensitive amplifiers may be obtained other than via a multiplexer.

[0025] The serial output may be supplied to a discriminator, for example a threshold level detector, whose binary output has first and second levels, representing the two possible states of the sensing elements, e.g. written or unwritten.

[0026] The timing of the transition between the aforementioned first and latter parts of the row selection period is determined by the control circuit 19 which supplies switching signals to the switches 48 and 51 so as to close the former and connect the non-inverting input of the amplifier to the output from the respective sample and hold stage of the data signal drive circuit 30 on which a data signal intended for the selected display element is present. Closure of the switch 48 serves to reset the capacitor 47 and connects the amplifier output directly with the column conductor 16. In this configuration the sense amplifier behaves as a unity gain buffer and the data signal present at the non-inverting input appears on the column conductor 16. Consequently, the LC element of the selected display element is charged according to the level of this data signal. Thus, the amplifier circuit 45 fulfills two roles, namely to act as a charge sensitive amplifier in a read operation to determine the state of the sensing element and to act as a buffer amplifier between the sample and hold circuit of the data signal drive circuit 30 and the column conductor 16 during the display element loading operation.

[0027] The other stages of the detection circuit 40 operate simultaneously in identical manner to read and load their sensing and display elements respectively in the same row.

[0028] Upon termination of the row selection signal to the row conductor the control circuit 19 opens the switch 48 and operates the switch 51 to connect the non-inverting input to the source of Vread. A row selection signal is then applied to the next row conductor 14 and the sequence of operations is repeated so as to read and load the sensing and display elements in this row. This operation is repeated for each row of sensing and display elements so that over the course of a display field period the conditions of all the sensing elements in the array are read and all the display elements are loaded with their respective data signals, the arrays being repeatedly addressed in this manner in successive fields.

[0029] As this embodiment is similar to that described in EP-A-0491436 except for particularly the configuration and manner of operation of the column drive/read circuit, it shares similar advantages. In particular, the sensing elements have a memory function so that an indication of a light input can be obtained after the event and the sensing and display elements share the same row and column address conductors which greatly simplifies construction. These and other advantages are discussed in EP-A-0491436.

[0030] Various modifications are possible as de-

scribed in EP-A-0491436, for example with regard to the components of the sensing elements and their circuit configuration.

[0031] The invention is not restricted to this particular kind of device, however, but can be applied to other kinds of combined matrix display and light sensing devices in which the light sensing elements are read using sense amplifiers and in which buffer amplifiers are required between a circuit supplying data signals for the display elements and the column address conductors.

[0032] Other kinds of combined matrix display and light sensing devices are known which rely on sensing of a light input simultaneously with the application of that input. In these devices a basic frame period is divided into a display frame interval during which all rows of display elements are addressed with display information followed by a light detection interval during which the conditions of the sensing elements are detected. Such temporally separate display and detection frames are avoided in the above-described embodiment. In other known devices separate sets of row and column address conductors are used for the display and sensing elements respectively, thus doubling the number of address conductors required assuming display and sensing elements are provided on a one to one basis.

[0033] Figure 4 illustrates a modification of the circuit configuration depicted in Figure 3 another embodiment in which the device comprises separate column address conductors for each column of sensing and display elements. The column conductors for the sensing elements and the display elements are designated 16' and 16" respectively. This circuit further includes switches 55 and 56 connected between the amplifier input and the sensing element column conductor 16' and the display element column conductor 16" respectively. A switching signal from the control circuit 19 is applied to the switch 55 and, through an inverter 57, to the switch 56 in synchronism with operation of the switches 48 and 51 so that when the switch 48 is open the switches 55 and 56 are closed and open respectively and the read potential Vread appears on the conductor 16' and when the switch 48 is closed the switches 55 and 56 are open and closed respectively such that the data signal Vd appears on the conductor 16".

[0034] Figure 5 illustrates schematically the circuit for an alternative form of sensing element, 18', and its connection to an associated sense amplifier circuit 45. The drain of the sensing element TFT 24 is connected to one side of a photodiode whose other terminal is connected to a supplementary row conductor 61 common to all sensing elements in the same row which is held at a predetermined reference potential Vs. Upon the application of a row selection signal to the row address conductor 14, and with the switch 48 of the charge sensitive amplifier circuit 45 open, charge is integrated on the capacitor 47 upon the photodiode being illuminated with a light input. The photodiode may be replaced by a photoresistor as depicted in dotted outline in Figure 5.

[0035] From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the field of matrix display and light sensing devices and which may be used instead of or in addition to features already described herein.

Claims

1. A combined matrix display and light sensing device comprising an array of display elements (12), an array of light sensing elements (18) which are responsive to illumination so as to provide an electrical charge indicative thereof, first and second sets of address conductors (14, 16) connected with the arrays of display and light sensing elements, the display elements and the light sensing elements each being connected with an address conductor of each set, a first drive circuit (15) connected to the first set of address conductors (14) for scanning the arrays, a second drive circuit (30) for providing data signals which are supplied to the display elements via address conductors (16) of the second set, a detection circuit (40) for sensing the charge provided by the sensing elements (18) and providing an output in accordance therewith and comprising charge sensitive amplifier circuits (45) each having an output, a first input connected to an address conductor (16) of the second set, a second input for receiving a read potential and a capacitor (47) and switch (48) connected in parallel between the output and the first input, and control means (19) for opening and closing the switch (48) of each charge sensitive amplifier circuit periodically and providing a read potential to the second input, characterised in that the control means (19) is operable to apply to the second input of each charge sensitive amplifier circuit (45) data signals from the second drive circuit (30) when the switch (48) is closed and said read potential when the switch is open.

2. A device according to Claim 1, characterised in that individual address conductors (16) of the second set are connected to display elements (12) and sensing elements (18) and in that the individual address conductors are each connected to the first input of a respective charge sensitive amplifier circuit (45).

3. A device according to Claim 1, characterised in that the sensing elements (18) and the display elements (12) are connected respectively to different address conductors (16) of the second set and in that the first input of each charge sensitive amplifier circuit (45) is connected to a respective pair of address conductors of the second set comprising one con-

nected to sensing elements and one connected to display elements via a change-over switch (55, 56) which is operable by the control means in synchronism with the switch of the charge sensitive amplifier circuit.

Patentansprüche

1. Kombinierte Matrix-Wiedergabe- und Lichtabtastanordnung mit einer Anordnung von Wiedergabeelementen (12), einer Anordnung von Lichtabtastelementen (18), die auf Beleuchtung reagieren zum Schaffen einer elektrischen Ladungsanzeige davon, wobei ein erster und ein zweiter Satz von Adressenleitern (14, 16) mit den Anordnungen von Wiedergabe- und Lichtabtastelementen verbunden sind, wobei die Wiedergabeelemente und die Lichtabtastelemente je mit einem Adressenleiter jedes Satzes verbunden sind, mit einer ersten Treiberschaltung (15), die mit dem ersten Satz von Adressenleitern (14) verbunden ist zum Abtasten der Anordnungen, mit einer zweiten Treiberschaltung (30) zum Schaffen von Datensignalen, die den Wiedergabeelementen über Adressenleiter (16) des zweiten Satzes zugeführt werden, mit einer Detektionsschaltung (40) zum Abtasten der von den Abtastelementen (18) gelieferten Ladung und zum Liefern eines entsprechenden Ausgangssignals und mit Ladungsverstärkerschaltungen (45), mit je einem Ausgang, einem ersten Eingang, der mit einem Adressenleiter (16) des zweiten Satzes verbunden ist, einem zweiten Eingang zum Empfangen eines Lesepotentials und einer Parellelschaltung eines Kondensators (47) und eines Schalters (48) zwischen dem Ausgang und dem ersten Eingang, und mit Steuermitteln (19) zum periodischen Öffnen und Schließen des Schalters (48) jeder ladungsempfindlichen Verstärkerschaltung und zum Liefern eines Lesepotentials zu dem zweiten Eingang, dadurch gekennzeichnet, dass die Steuermittel (19) dem zweiten Eingang jeder ladungsempfindlichen Verstärkerschaltung (45) Datensignale von der zweiten Treiberschaltung (30) zuführen, wenn der Schalter (48) geschlossen ist und das genannte Lesepotential, wenn der Schalter offen ist.

2. Schaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, dass einzelne Adressenleiter (16) des zweiten Satzes mit Wiedergabeelementen (12) und Abtastelementen (18) verbunden sind und dass die einzelnen Adressenleiter je mit dem ersten Eingang einer betreffenden ladungsempfindlichen Verstärkerschaltung (45) verbunden sind.

3. Schaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, dass die Abtastelemente (18) und die Wiedergabeelemente (12) mit verschiedenen Adressenleitern (16) des zweiten Satzes verbunden sind und dass der erste Eingang jeder ladungsempfindlichen Verstärkerschaltung (45) mit einem betreffenden Paar von Adressenleitern des zweiten Satzes verbunden ist, wobei der eine mit den Abtastelementen und der andere über einen Umschalter (55, 56) mit den Wiedergabeelementen verbunden ist, wobei dieser Umschalter synchron zu dem Schalter der ladungsempfindlichen Verstärkerschaltung betrieben wird.

Revendications

1. Dispositif d'affichage matriciel et de détection optique combiné comprenant une matrice d'éléments d'affichage (12), une matrice d'éléments de détection optique (18) qui réagissent à une illumination de manière à fournir une charge électrique indicative de celle-ci, des premier et deuxième jeux de conducteurs d'adressage (14, 16) connectés aux matrices d'éléments d'affichage et de détection optique, chacun des éléments d'affichage et des éléments de détection optique étant connecté à un conducteur d'adressage de chaque jeu, un premier circuit d'attaque (15) étant connecté au premier jeu de conducteurs d'adressage (14) pour balayer les matrices, un deuxième circuit d'attaque (30) prévu pour fournir des signaux de données qui sont fournis aux éléments d'affichage par le biais des conducteurs d'adressage (16) du deuxième jeu, un circuit de détection (40) pour détecter la charge fournie par les éléments de détection (18) et fournissant une sortie en fonction de celle-ci et comprenant des circuits amplificateurs sensibles à la charge (45) comportant chacun une sortie, une première entrée connectée à un conducteur d'adressage (16) du deuxième jeu, une deuxième entrée pour recevoir un potentiel de lecture et un condensateur (47) et un commutateur (48) montés en parallèle entre la sortie et la première entrée, et un moyen de commande (19) pour ouvrir et fermer périodiquement le commutateur (48) de chaque circuit amplificateur sensible à la charge et fournir un potentiel de lecture à la deuxième entrée, caractérisé en ce que le moyen de commande (19) est activé pour appliquer à la deuxième entrée de chaque circuit amplificateur sensible à la charge (45) des signaux de données provenant du deuxième circuit d'attaque (30) lorsque le commutateur (48) est fermé et ledit potentiel de lecture lorsque le commutateur est ouvert.

2. Dispositif suivant la revendication 1, caractérisé en ce que des conducteurs d'adressage individuels (16) du deuxième jeu sont connectés à des éléments d'affichage (12) et des éléments de détection (18), et en ce que chacun des conducteurs d'adressage individuels est connecté à la première entrée

d'un circuit amplificateur sensible à la charge respectif (45).

3. Dispositif suivant la revendication 1, caractérisé en ce que les éléments de détection (18) et les éléments d'affichage (12) sont connectés respectivement à différents conducteurs d'adressage (16) du deuxième jeu, et en ce que la première entrée de chaque circuit amplificateur sensible à la charge (45) est connectée à une paire respective de conducteurs d'adressage du deuxième jeu comprenant un conducteur connecté aux éléments de détection et un conducteur connecté aux éléments d'affichage par l'intermédiaire d'un commutateur inverseur (55, 56) qui est activé par le moyen de commande en synchronisme avec le commutateur du circuit amplificateur sensible à la charge.

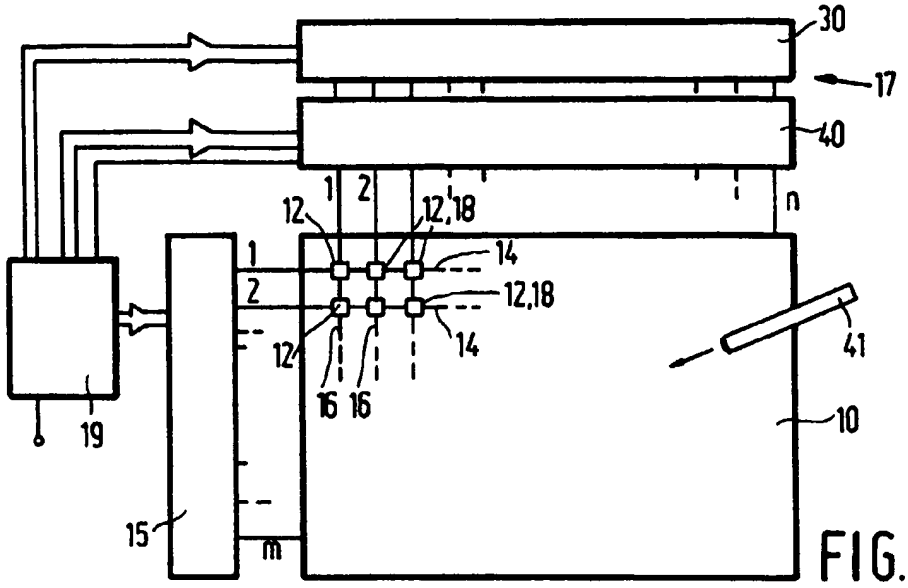

FIG.1

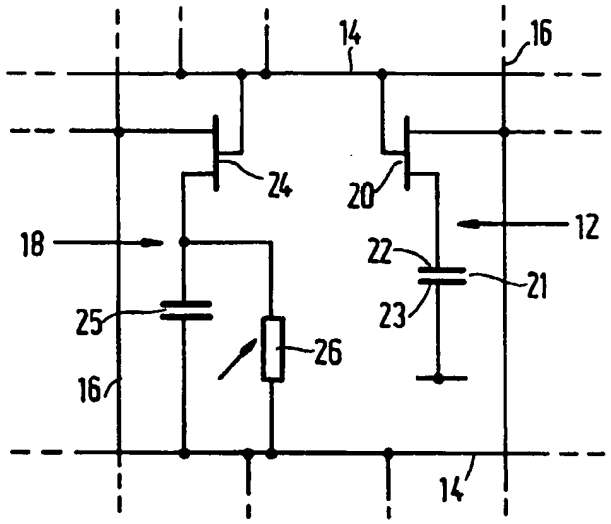

FIG.2

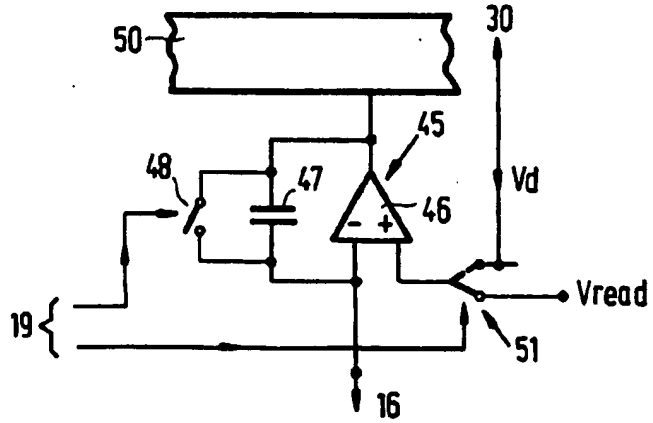

FIG.3

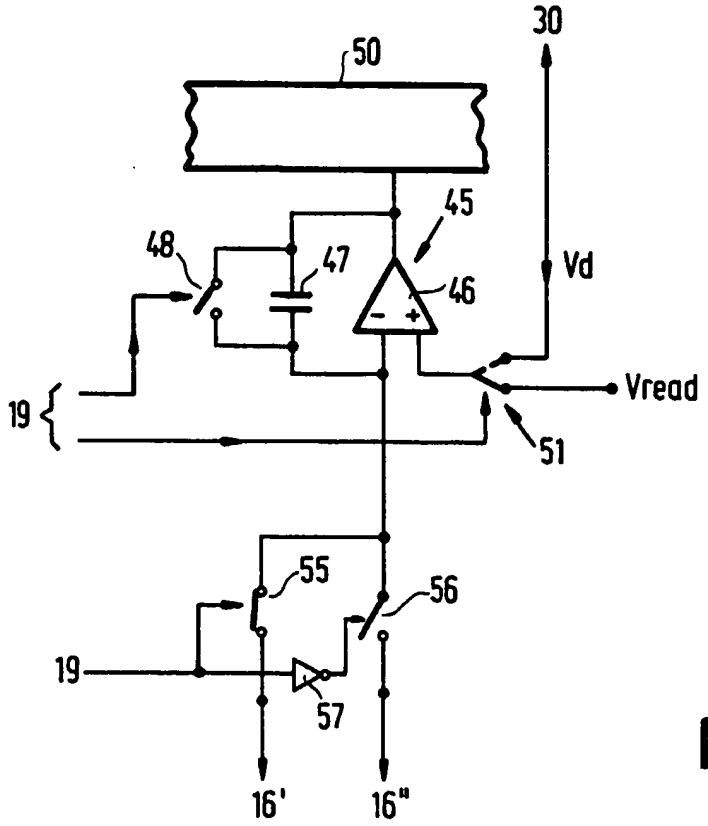
30
50
45
48
47
46
Vd
Vread
19
51
55
56
19
57
16'
16"

FIG. 4

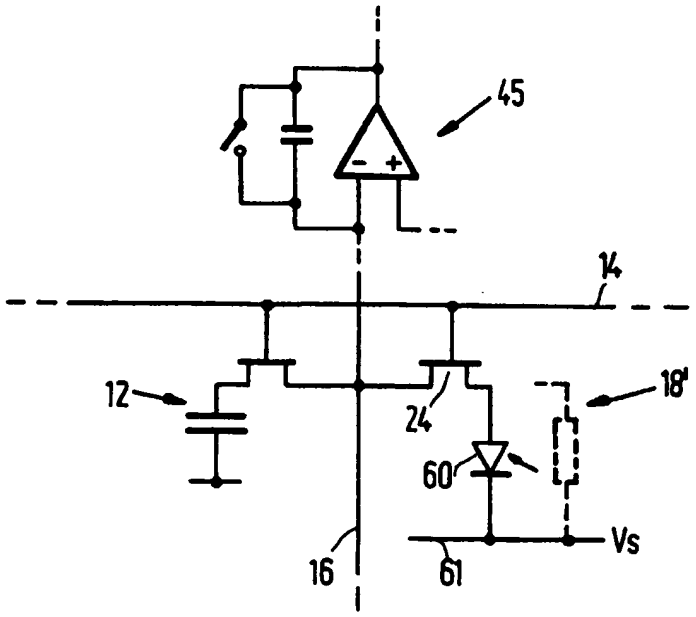
45
14
12
24
18'
60
Vs
16
61

FIG. 5